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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/871,805	06/04/2001	Shunpei Yamazaki	12732-049001	1978

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EXAMINER	
DONG, DALEI	

ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/871,805	YAMAZAKI, SHUNPEI	
	Examiner	Art Unit	
	Dalei Dong	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 5-15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,072,278 to Keyser in view of O'Brien et al. ("Improved Energy transfer in electrophosphorescent devices", Applied Physics Letters, 1999) in further view of Baldo et. al. ("Very high-efficiency green organic light-emitting devices based on electrophosphorescence", Applied Physics Letters, 1999) and yet in further view of U.S. Patent No. 6,191,764 to Kono.

Regarding to claim 1, 5-15 and 19, Keyser discloses in Figure 3, "an electroluminescent (EL) structure is shown and referred to generally as structure 100. A substrate 102 is provided for fabricating an increased capacitance EL pixel electrode structure. Substrate 102 is preferably silicon although other suitable materials are contemplated. Devices 107 for control circuitry as described above are included on a device layer 106 and include blocking transistors 130 (switching thin film transistor) and access transistors 132 (current control thin film transistor) (shown in FIG. 4)" (column 5, line 41-48).

Keyser also discloses in Figure 3, "an insulating layer 104 is formed on substrate 102 to isolate devices formed thereon from substrate 102. Insulating layer is preferably formed from silicon dioxide or equivalent materials. Device layer 106 is formed on insulating layer 104. Device layer 106 is preferably silicon. Devices 107 include transistors or other semiconductor devices. Transistors and capacitors comprise the control circuitry for activating pixel electrode 116 as described above with reference to FIG. 2" (column 5, line 49-58).

Keyser further discloses in Figure 3, "a dielectric layer 126 is formed on device layer 106. A conductive layer 110 is deposited on dielectric layer 126. Conductive layer 110 forms a first electrode 108 for a hold capacitor 109. Electrode 108 connects to a gate of a blocking transistor 130 (FIG. 4) used to activate pixel electrode 116. Electrode 108 also connects to one end of access transistor 32 (FIG. 2). A high dielectric constant layer 124 is deposited over an entire surface of structure 100 on conductive layer 110 and another conductive layer 112 is formed on dielectric layer 124. A portion of conductive layer 112 forms a second electrode 111 of hold capacitor 109. In one embodiment, conductive layer 112 can function as a capacitor plate and/or a high voltage shield to protect controlling transistors from phosphor (EL) excitation signals. Conductive layer 112 connects to control circuitry, for example, a transistor source, such as blocking transistor 130 (FIG. 4) source to tie it to ground" (column 5, line 59-67 to column 6, line 1-8).

Keyser further yet discloses in Figure 3, "an interlevel dielectric layer 122 is deposited to isolate the control circuitry from pixel electrode 116. Dielectric layer 122 is

then planarized using established chemical-mechanical polishing (CMP) or by providing a sacrificial layer and etching it back to provide a planarized surface for the formation of additional layers as described hereinafter. Vias 114 and 1 15 connect a drain of blocking transistor 130 (FIG. 4) in device layer 106 to electrode 116" (column 6, line 9-16).

Keyser further yet discloses in Figure 3, "an electroluminescent stack 118 and a transparent electrode 120 are formed continuously across a surface of the structure 100. Electroluminescent stack 118 may include a dielectric layer above and below it to isolate electroluminescent layer 118 from pixel electrode 116 and transparent electrode 120, respectively. Electroluminescent stack 118 preferably includes zinc sulfide, strontium sulfide or organic materials. For organic materials, electroluminescent stack 118 does not include dielectric layers above and below it, instead an electron transport layer and a hole transport layer sandwich an organic electroluminescent layer" (column 6, line 17-27).

However, Keyser does not disclose different pixel of the EL structure emitting different color of light and wherein a triplet compound is used in the first EL element while a singlet compound is used in the second and third EL element. O'Brien teaches triplet compound of PtOEP, however fails to teach a singlet compound. Baldo teaches a singlet compound of $Ir(ppy)_3$.

Kono further teaches that is old and well known in the art to utilize both triplet and singlet excitons in an electroluminescent device "the current that flows between the first address electrodes 20 and the second address electrodes 22 causes electrons and holes to be recombined inside the organic electroluminescent layer 21, generating singlet excitons to triplet excitons, so that the address organic electroluminescent layer 21 emits

light of a predetermined wavelength range corresponding to the material or the like of the layer 21. The first address electrodes 20 has such a property as to pass at least the light component of the wavelength range, included in the light from the organic electroluminescent layer 21, which excites the base of the bipolar phototransistor 16 to generate electrons and holes in the base. The transparent substrate 14 and the transparent electrode 15 both also have such a property as to pass at least the light component of the wavelength range, included in the light from the organic electroluminescent layer 21, which excites the base of the bipolar phototransistor 16 to generate electrons and holes in the base" (column 3, lines 59 to column 4, line 9).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilize the triplet PtOEP electrophosphorescence material of O'Brien and the singlet $Ir(ppy)_3$ electrophosphorescent material of Baldo within single electroluminescent structure of Keyser according to Kono in order to provide an electroluminscent display having a plurality of high-performance pixels with significantly enhanced bright color and contrast ratio and further uniform the light intensity from each pixels.

3. Claims 2-4, 16-18 and 20-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,932,892 to Hseuh in view of O'Brien et al. ("Improved Energy transfer in electrophosphorescent devices", Applied Physics Letters, 1999) and yet in further view of Baldo et. al. ("Very high-efficiency green organic light-emitting devices

based on electrophosphorescence", Applied Physics Letters, 1999) and yet in further view of U.S. Patent No. 6,191,764 to Kono.

Regarding to claims 2, 16 and 20-30, Hseuh discloses in Figure 1, "the AMELD pixel 102, the switching circuit 106 contains a pair of transistors 110 *switching thin film transistor* and 112 *current control thin film transistor* that are switchable using a select line 114 and a data line 116. To form circuit 106, transistor 110, typically a low voltage metal oxide semiconductor (MOS) transistor, has its gate connected to the select line 114, its source connected to the data line 116, and its drain connected to the gate of the second transistor 112 and through a first capacitor 118 to the electric field shield 104. The electric field shield is connected to ground. Importantly, as shall be discussed in detail below, the first capacitor is actually manifested as the capacitance between the shield 104 and the gate electrode of transistor 112. To complete the switching circuit, transistor 112, typically a high voltage MOS transistor, has its source connected to the data line 116 and its drain connected to one electrode of the EL cell 108. A high voltage bus 122 connects the second electrode of the EL cell to a high voltage (e.g., 250 volts) alternating current (AC) source 120" (column 2, line 62 to column 3, line 12).

Heeuh also discloses in Figure 1, "the transistors used to form the switching circuit 106 may be of any one of a number of designs. Typically, the first transistor is a low breakdown voltage (less than 10 volts) MOS transistor. The second transistor is typically a double diffused MOS (DMOS) device having a high breakdown voltage (greater than 150 volts). The transistors can be either n- or p-channel devices or a

combination thereof, e.g., two NMOS transistors, two PMOS transistors or a combination of NMOS and PMOS transistors" (column 3, line 13-21).

Hseuh further discloses in Figure 1, "images are displayed on the AMELD as a sequence of frames, in either an interlace or progressive scan mode. During an individual scan, the frame time is sub-divided into a separate LOAD period and an ILLUMINATE period. During the LOAD period, an analog-to-digital converter 124 and a low impedance buffer 126 produce data for storage in the switching circuitry. The data is loaded from the data line 116 through transistor 110 and stored in capacitor 118. Specifically, the data lines are sequentially activated one at a time for the entire display. During activation of a particular data line, a select number of select lines are activated (strobed). Any transistor 110, located at the junction of activated data and select lines, is turned ON and, as such, the voltage on the data line charges the gate of transistor 112. This charge is primarily stored in a capacitance between the gate and the electric field shield (represented as capacitor 118). This charge storage is discussed in detail with regard to FIG. 2L. As the charge accumulates on the gate of transistor 112, the transistor begins conduction, i.e., is turned ON. At the completion of the LOAD period, the high voltage transistor in each pixel that is intended to be illuminated is turned ON. As such, during the ILLUMINATE period, the high voltage AC source that is connected to all the pixels in the display through bus 122 is activated and simultaneously applies the AC voltage to all the pixels. However, current flows from the AC source through the EL cell and the transistor 112 to the data line 116 in only those pixels having an activated transistor 112. Consequently, during the ILLUMINATE period of each frame, the active

pixels produce electroluminescent light from their associated EL cells" (column 3, lines 32-62).

However, Hseuh fails to teach different pixel of the EL structure emitting different color of light and wherein a triplet compound is used in the first EL element while a singlet compound is used in the second and third EL element. O'Brien teaches triplet compound of PtOEP, however fails to teach a singlet compound. Baldo teaches a singlet compound of $Ir(ppy)_3$.

Kono further teaches that is old and well known in the art to utilize both triplet and singlet excitons in an electroluminescent device "the current that flows between the first address electrodes 20 and the second address electrodes 22 causes electrons and holes to be recombined inside the organic electroluminescent layer 21, generating singlet excitons to triplet excitons, so that the address organic electroluminescent layer 21 emits light of a predetermined wavelength range corresponding to the material or the like of the layer 21. The first address electrodes 20 has such a property as to pass at least the light component of the wavelength range, included in the light from the organic electroluminescent layer 21, which excites the base of the bipolar phototransistor 16 to generate electrons and holes in the base. The transparent substrate 14 and the transparent electrode 15 both also have such a property as to pass at least the light component of the wavelength range, included in the light from the organic electroluminescent layer 21, which excites the base of the bipolar phototransistor 16 to generate electrons and holes in the base" (column 3, lines 59 to column 4, line 9).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilize the triplet PtOEP electrophosphorescence material of O'Brien and the singlet $Ir(ppy)_3$ electrophosphorescent material of Baldo within a single electroluminescent structure of Hseuh according to Kono and construct the switching and controlling thin film transistor of Hseuh using either n-channel or p-channel interchangeably in order to provide an electroluminscent display having a plurality of high-performance pixels with significantly enhanced bright color and contrast and thus uniform the light intensity from each pixels and furthermore, eliminate the error in activation display device and upgrade the controllability of the display device.

Regarding to claims 3, 17 and 31-41, Hseuh discloses in Figure 1, "the AMELD pixel 102, the switching circuit 106 contains a pair of transistors 110 *switching thin film transistor* and 112 *current control thin film transistor* that are switchable using a select line 114 and a data line 116. To form circuit 106, transistor 110, typically a low voltage metal oxide semiconductor (MOS) transistor, has its gate connected to the select line 114, its source connected to the data line 116, and its drain connected to the gate of the second transistor 112 and through a first capacitor 118 to the electric field shield 104. The electric field shield is connected to ground. Importantly, as shall be discussed in detail below, the first capacitor is actually manifested as the capacitance between the shield 104 and the gate electrode of transistor 112. To complete the switching circuit, transistor 112, typically a high voltage MOS transistor, has its source connected to the data line 116 and its drain connected to one electrode of the EL cell 108. A high voltage bus 122 connects

the second electrode of the EL cell to a high voltage (e.g., 250 volts) alternating current (AC) source 120" (column 2, line 62 to column 3, line 12).

Heeuh also discloses in Figure 1, "the transistors used to form the switching circuit 106 may be of any one of a number of designs. Typically, the first transistor is a low breakdown voltage (less than 10 volts) MOS transistor. The second transistor is typically a double diffused MOS (DMOS) device having a high breakdown voltage (greater than 150 volts). The transistors can be either n- or p-channel devices or a combination thereof, e.g., two NMOS transistors, two PMOS transistors or a combination of NMOS and PMOS transistors" (column 3, line 13-21).

Hseuh further discloses in Figure 1, "images are displayed on the AMELD as a sequence of frames, in either an interlace or progressive scan mode. During an individual scan, the frame time is sub-divided into a separate LOAD period and an ILLUMINATE period. During the LOAD period, an analog-to-digital converter 124 and a low impedance buffer 126 produce data for storage in the switching circuitry. The data is loaded from the data line 116 through transistor 110 and stored in capacitor 118. Specifically, the data lines are sequentially activated one at a time for the entire display. During activation of a particular data line, a select number of select lines are activated (strobed). Any transistor 110, located at the junction of activated data and select lines, is turned ON and, as such, the voltage on the data line charges the gate of transistor 112. This charge is primarily stored in a capacitance between the gate and the electric field shield (represented as capacitor 118). This charge storage is discussed in detail with regard to FIG. 2L. As the charge accumulates on the gate of transistor 112, the transistor

begins conduction, i.e., is turned ON. At the completion of the LOAD period, the high voltage transistor in each pixel that is intended to be illuminated is turned ON. As such, during the ILLUMINATE period, the high voltage AC source that is connected to all the pixels in the display through bus 122 is activated and simultaneously applies the AC voltage to all the pixels. However, current flows from the AC source through the EL cell and the transistor 112 to the data line 116 in only those pixels having an activated transistor 112. Consequently, during the ILLUMINATE period of each frame, the active pixels produce electroluminescent light from their associated EL cells" (column 3, lines 32-62).

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electroluminescent layer 21, which excites the base of the bipolar phototransistor 16 to generate electrons and holes in the base. The transparent substrate 14 and the transparent electrode 15 both also have such a property as to pass at least the light component of the wavelength range, included in the light from the organic electroluminescent layer 21, which excites the base of the bipolar phototransistor 16 to generate electrons and holes in the base" (column 3, lines 59 to column 4, line 9).

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Regarding to claims 4, 18 and 42-52, Hseuh discloses in Figure 1, "the AMELD pixel 102, the switching circuit 106 contains a pair of transistors 110 *switching thin film transistor* and 112 *current control thin film transistor* that are switchable using a select line 114 and a data line 116. To form circuit 106, transistor 110, typically a low voltage metal oxide semiconductor (MOS) transistor, has its gate connected to the select line 114, its source connected to the data line 116, and its drain connected to the gate of the second

transistor 112 and through a first capacitor 118 to the electric field shield 104. The electric field shield is connected to ground. Importantly, as shall be discussed in detail below, the first capacitor is actually manifested as the capacitance between the shield 104 and the gate electrode of transistor 112. To complete the switching circuit, transistor 112, typically a high voltage MOS transistor, has its source connected to the data line 116 and its drain connected to one electrode of the EL cell 108. A high voltage bus 122 connects the second electrode of the EL cell to a high voltage (e.g., 250 volts) alternating current (AC) source 120" (column 2, line 62 to column 3, line 12).

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Response to Arguments

4. Applicant's arguments with respect to claims 1-52 have been considered but are moot in view of the new ground(s) of rejection.

In response to Applicant's argument that the prior art of record fails to teach or suggest using a triplet compounding for emitting a red light and using a singlet compound for emitting a green light and a blue light. Examiner asserts that O'Brien reference clearly teaches that it is old and well known in the art to utilize a triplet compound for emitting a red light where "previous work on the red phosphor 2,3,7,8,12,13,17,18-octaethyle-21H, 23H-porphine platinum (II) PtOEP" (first paragraph). Further, Baldo reference teaches that it is old and well known in the art to utilize a singlet compound to emitting green and blue light wherein "OLEDs employing the green, electrophosphorescent material fac tris(2-phenylpyridine) iridium [$Ir(ppy)_3$]" (first paragraph). Baldo reference furthermore teaches "base on this assumption, the blue (λ - 400nm peak) emissive material 4,4'-N,N'-dicarbazole-bipheny (CBP) was chosen as the host for [$Ir(ppy)_3$]" (fourth paragraph). Thus, Examiner asserts that the prior art of record teaches the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dalei Dong whose telephone number is (571)272-2370. The examiner can normally be reached on 8 A.M. to 5 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar Patel can be reached on (571)272-2457. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D.D.
April 27, 2004

VIP PATEL
PRIMARY EXAMINER